

Fig.1

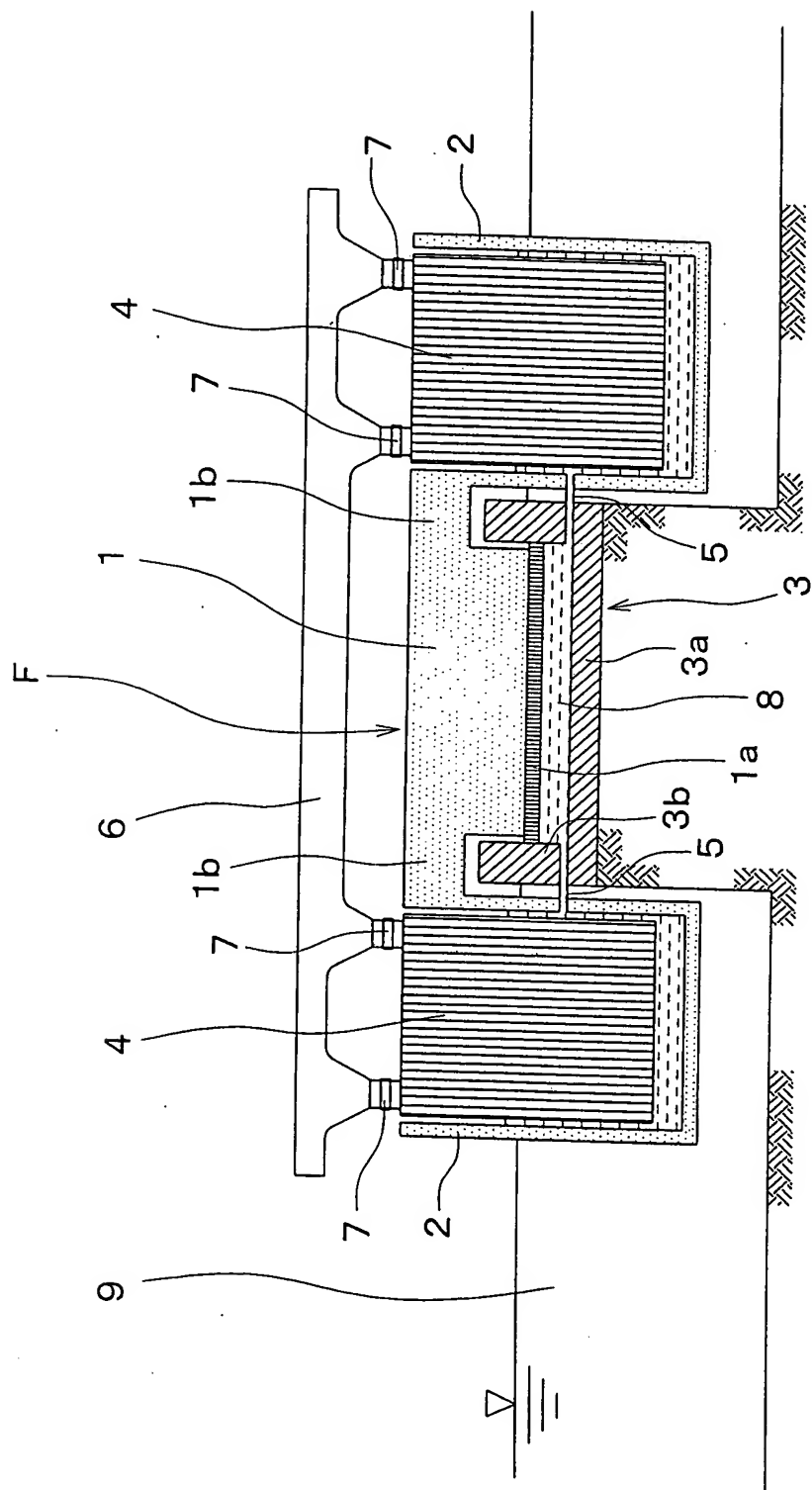


Fig.2

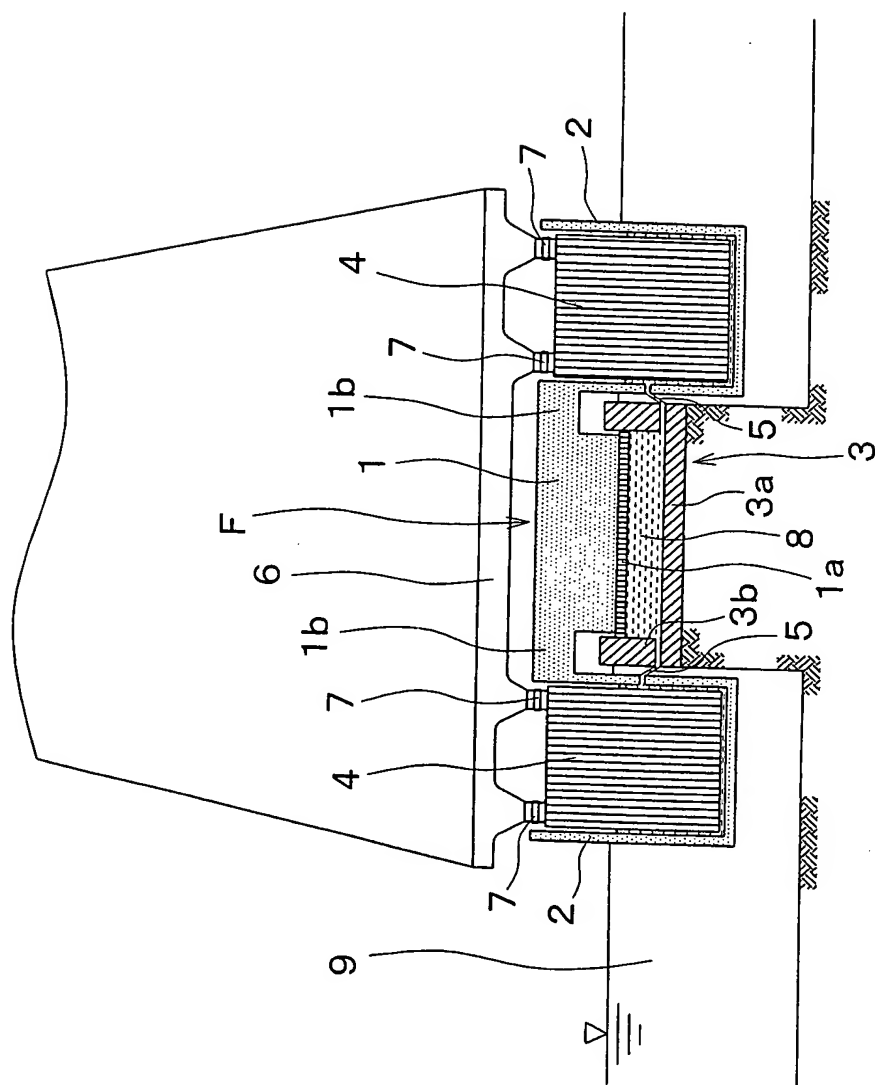


Fig. 1 is a cross-sectional view of a semiconductor device. It shows a substrate 1 with a central channel 1a and side regions 1b. Two gate structures 2 are positioned on either side of the channel, each containing a gate 4 and a series of vertical gates 7. A source/drain region 3 is located between the gates, featuring a contact layer 5 and a conductive pad 8. A passivation layer 6 covers the top surface of the device. A bond wire 9 is connected to a pad 13 on the top surface.

Fig.4

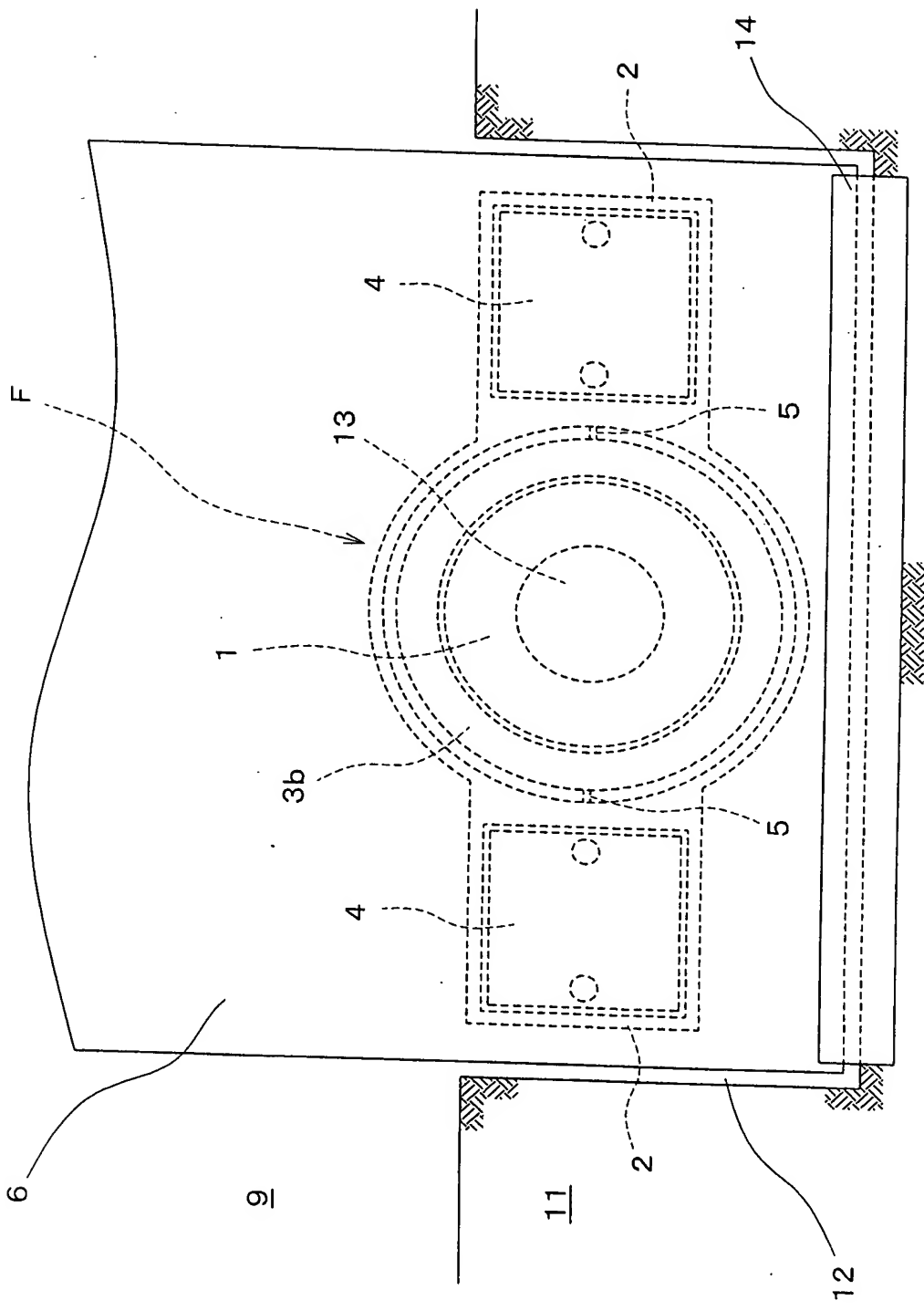
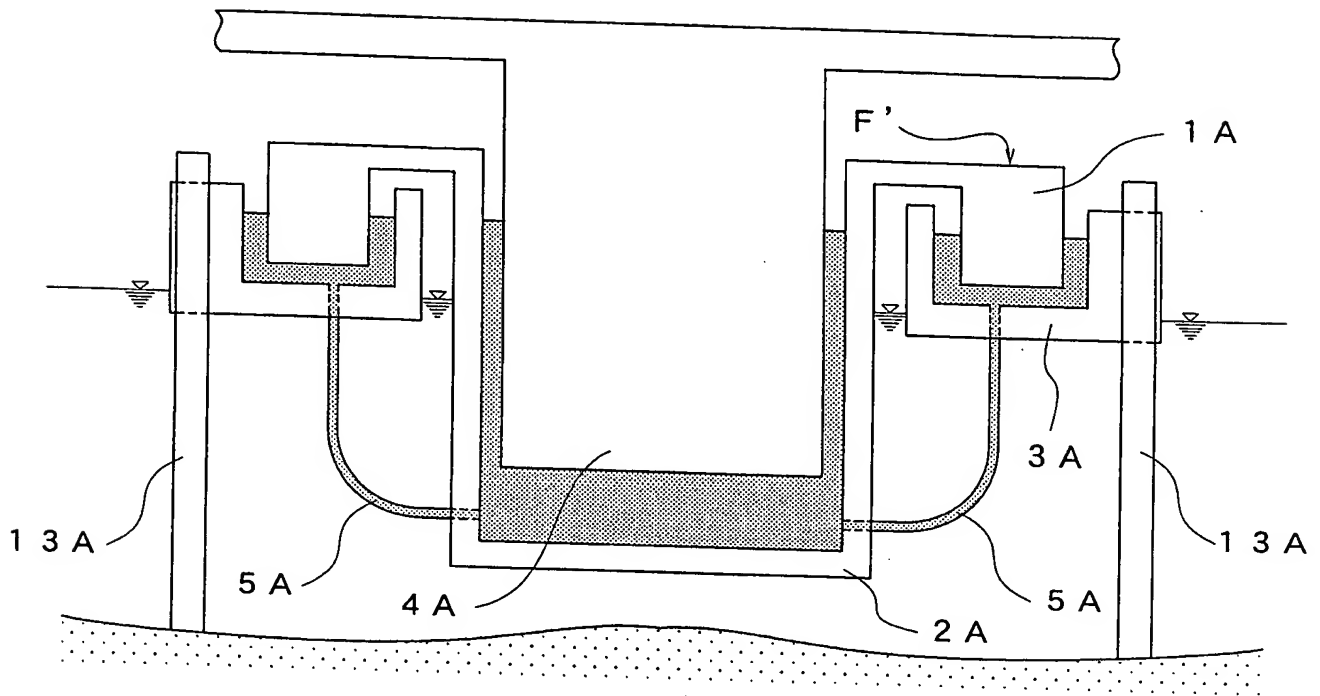


Fig. 5

(a)



(b)

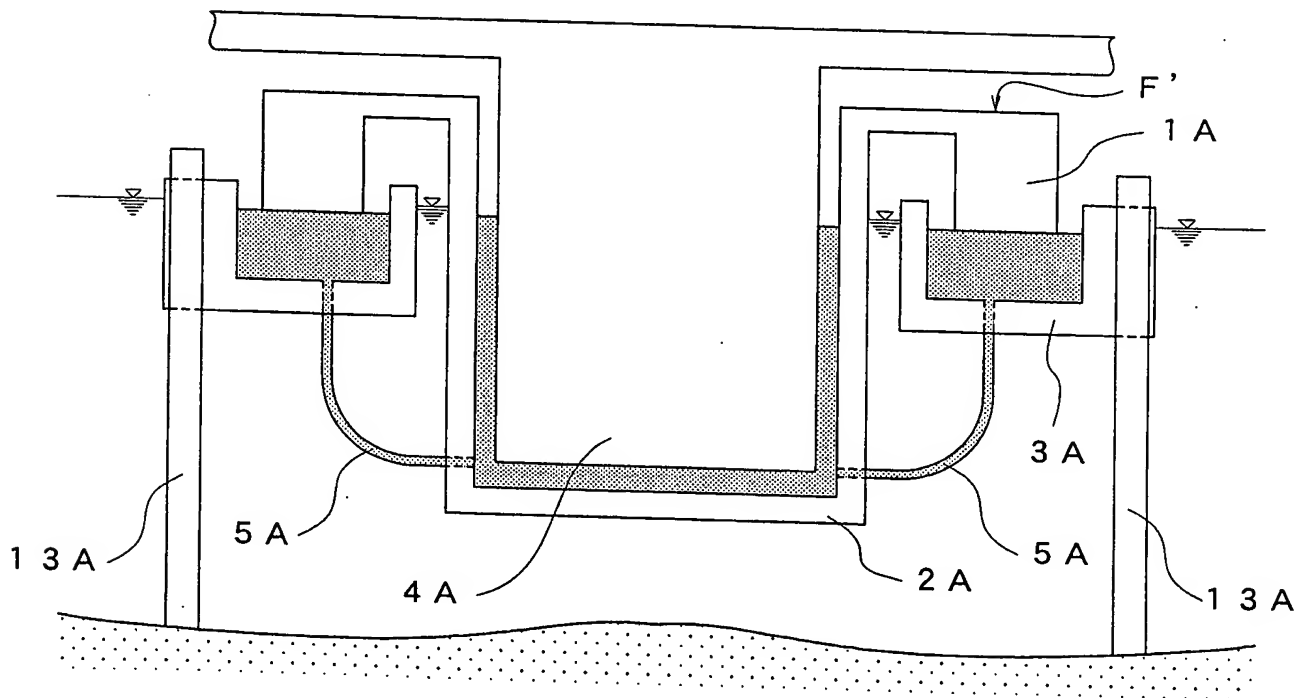


Fig. 6

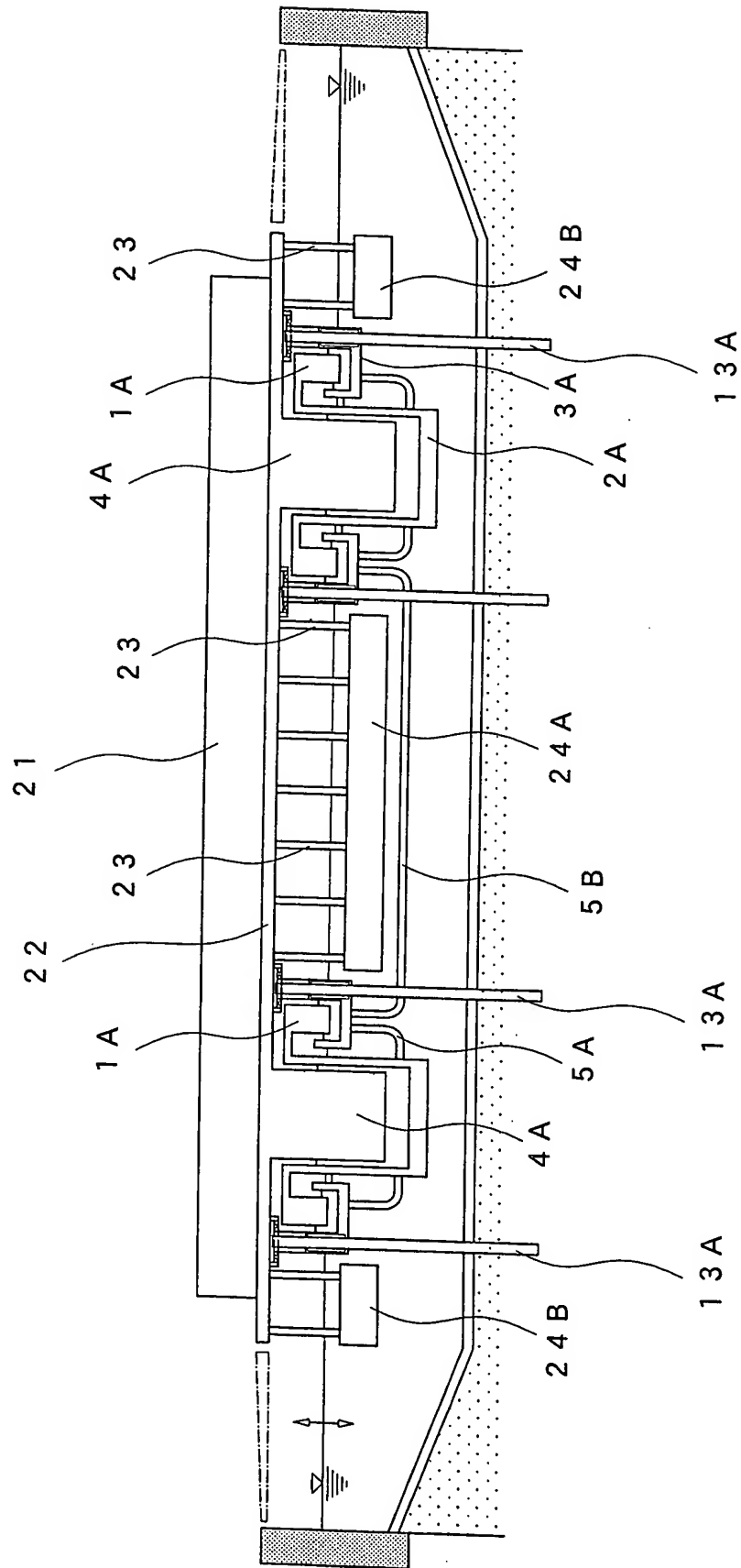


Fig. 7

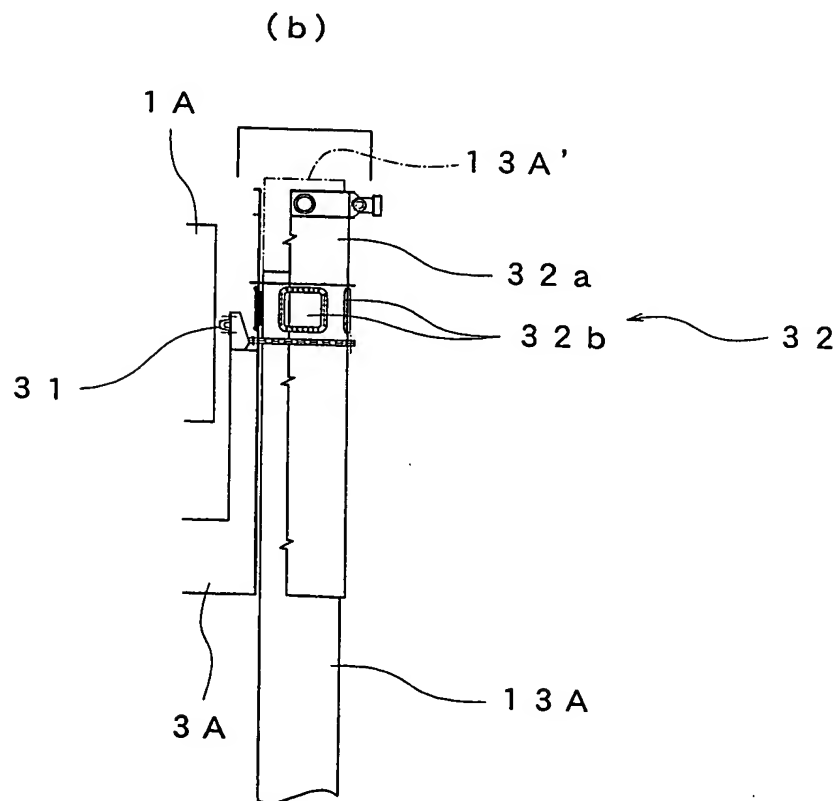
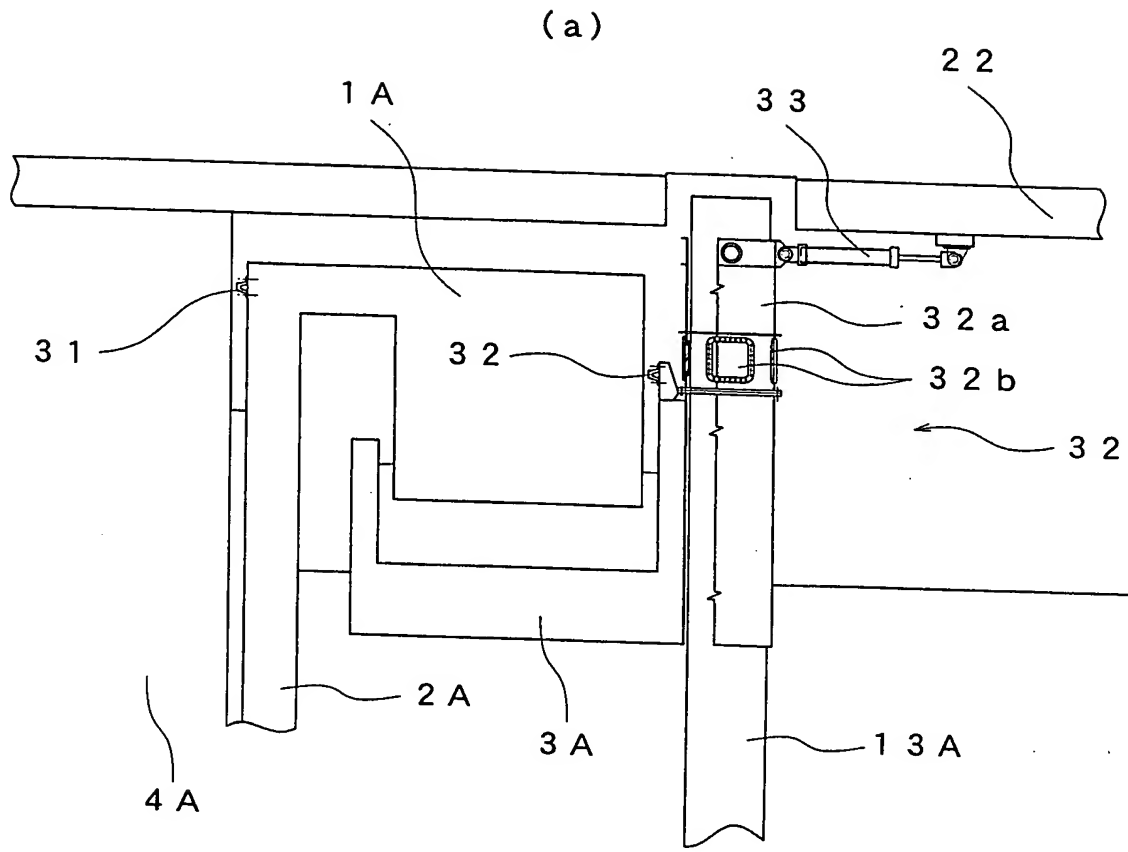


Fig. 8

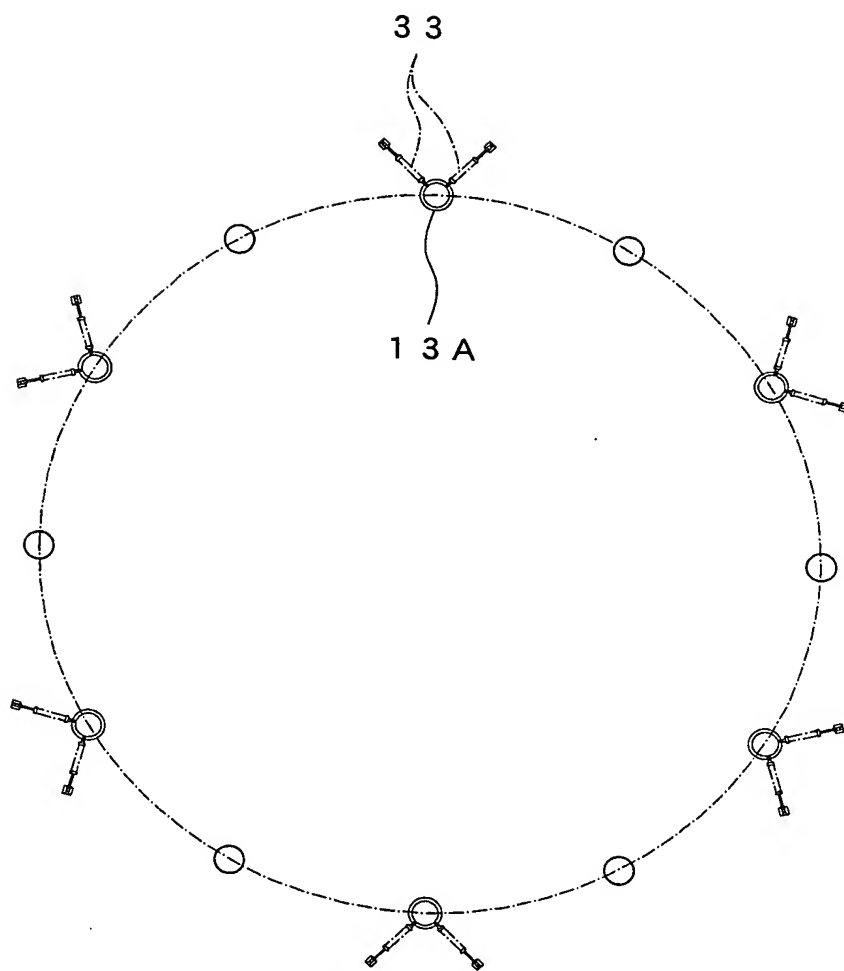




Fig. 9

